Taiwan Publication No. 340297 (Application No. 86103176)
Title: Packaging Method for a Ball Grid Array Integrated Circuit without Utilizing a Base Plate and Solder Balls
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ABSTRACT

The present invention relates to a packaging method for a ball grid array (BGA) integrated circuit (IC), more particularly to a packaging method for a BGA IC without utilizing a lead frame as a base plate and without implanting solder balls, thereby allowing a packaged IC to have a very small thickness and avoiding insufficient strength due to solder balls. The method comprises the steps of: covering a copper sheet with a first patterned dry film; slightly etching the surface of the copper sheet to form recesses that will provide external contact positions of the BGA IC; electroplating the recesses with metal to form a first electroplated layer; removing the first dry film; covering the top of the copper sheet with a second patterned dry film; electroplating the top of the copper sheet with metal to form a second electroplated layer that corresponds to internal contact positions of the BGA IC; covering the top of the resulting structure with a third patterned dry film that exposes a desired bond pad area; electroplating the bond pad area with metal to form a third electroplated layer; removing the second and third dry films; implanting an IC chip; drawing wires; sealing the chip and the wires with a resin; etching the copper sheet; and covering the bottom of the resulting structure with a patterned green paint, thereby packaging the BGA IC and utilizing the first electroplated layer as the external contact positions and without utilizing a base plate therein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a packaging method for a ball grid array (BGA) integrated circuit (IC), more particularly to a packaging method for a BGA IC without utilizing a base plate and solder balls, thereby allowing a packaged IC to have a very small thickness and an improved structural strength.

2. Description of Related Art

Nowadays, there are various methods for packaging ICs, e.g. DIP, PGA, BGA,

TAB, etc. in different applications. With respect to BGA (ball grid array), An array of solder balls as contact positions are disposed on the bottom of an IC package, which will be correspondingly soldered to contact positions on a printed circuit board. In a conventional BGA packaging method, however, it is necessary to provide a base plate as a supporting plate to carry the chip and the solder balls. Such a packaged IC with a base plate has a considerable thickness, thereby occupying a sizable space when being applied to a small-sized device such as a notebook computer or a sub-notebook computer. Further, because of insufficient strength provided by the solder balls that are additionally attached to the bottom, the solder balls may be easily detached from the packaged IC in tension.

SUMMARY OF THE INVENTION

One objective of the present invention is to provide an improved packaging method for a BGA IC without utilizing a base plate as a supporting plate, therefore reducing the thickness of the packaged BGA IC.

Another objective of the present invention is to provide an improved packaging method for a BGA IC without utilizing solder balls that are additionally attached, therefore enhancing the strength at the contact positions of the packaged BGA IC.

In accordance with the present invention, the packaging method for a BGA IC comprises the steps of: covering a copper sheet with a first patterned dry film; slightly etching the surface of the copper sheet to form recesses that will provide external contact positions of the BGA IC; electroplating the recesses with metal to form a first electroplated layer covering the recesses; removing the first dry film; covering the top of the copper sheet with a second patterned dry film; electroplating the top of the copper sheet with metal to form a second electroplated layer that corresponds to internal contact positions of the BGA IC; covering the top of the resulting structure with a third patterned dry film that exposes a desired bond pad area; electroplating the bond pad area with metal to form a third electroplated layer; removing the second and third dry films; implanting the IC chip; drawing wires; sealing the chip and the wires with a resin; etching the copper sheet to expose the bottoms of the recesses that are the downward protrusions of the first electroplated layer; and covering the bottom of the resulting structure with a patterned green paint.

Other objectives, advantages and novel features of the invention will become more

apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1K are schematic cross-sectional views illustrating the steps of the packaging method for a BGA IC in accordance with the present invention, wherein:

Fig. 1A: slightly etching to form recesses;

Fig. 1B: electroplating the recesses with nickel, gold, nickel and tin;

Fig. 1C: removing the first dry film;

Fig. 1D: electroplating the circuit areas with nickel, copper and gold;

Fig. 1E: applying the third dry film;

Fig. 1F: electroplating the bond pad area with gold;

Fig. 1G: removing the second and third dry films;

Fig. 1H: implanting a chip and drawing wires;

Fig. 1I: resin sealing;

Fig. 1J: etching the copper sheet and applying the green paint; and

Fig. 1K: removing nickel.

REFERENCE NUMERALS OF THE ELEMENTS IN THE DRAWINGS

10	copper sheet
11	recess
20	first dry film
30	first electroplated layer
40	second dry film
41	third dry film
50	second electroplated layer
52	third electroplated layer
60	IC chip
61	gold wire
70	protective resin
80	green paint
90	silver paste

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

A preferred embodiment illustrating the steps of the packaging method for a BGA IC in accordance with the present invention will be described in detail with reference to the accompanying drawings.

With Reference to Fig. 1A, a copper sheet 10 is covered with a first patterned dry film 20 that will assist in forming external contact positions of a BGA IC. The dry film 20 is patterned by exposure/development techniques well known in the art. With the first patterned dry film 20 as a mask, the surface of the copper sheet 10 uncovered with the first patterned dry film 20 is then slightly etched to form substantially round recesses 11 in the copper sheet 10. The positions of these recesses 11 correspond to the external contact positions of the BGA IC.

Still with the first patterned dry film 20 as a mask, the recesses 11 are electroplated in sequence with nickel, gold, nickel and tin to form a first electroplated layer 30 to cover the recesses 11, as shown in Fig. 1B. Thus, the first electroplated layer 30 can be regarded as a combination of several sub-layers. The first dry film 20 is then removed, as shown in Fig. 1C.

With Reference to Fig. 1D, the top of the copper sheet 10 is covered with a second patterned dry film 40 that corresponds to desired circuit areas and exposes the central portion of the copper sheet 10 and all of the first electroplated layer 30. With the second patterned dry film 40 as a mask, the central portion of the copper sheet 10 and all of the first electroplated layer 30 are then electroplated with nickel, copper and gold to form a second electroplated layer 50 that corresponds to internal contact positions of the BGA IC.

The top of the resulting structure is further covered with a third patterned dry film 41 that exposes a desired bond pad area, as shown in Fig. 1E. With the third patterned dry film 41 as a mask, the bond pad area is then electroplated with gold to form a third electroplated layer 52, as shown in Fig. 1F.

As shown in Fig. 1G, the second and third dry films 40 and 41 are removed, leaving the second and third electroplated layers 50 and 52 as well as the first electroplated layer 30 in the recesses 11 of the copper sheet 10.

With Reference to Fig. 1H, an IC or LSI chip 60 is implanted onto the central

portion of the copper sheet 10 that was previously covered with a silver paste 90. The terminals of the chip 60 are electrically connected with the bond pad area by gold wires 61. For example, gold wires 61 are drawn between the chip 60 and the third electroplated layer 52 in the bond pad area.

The chip 60 and the gold wires 61 are then sealed with a protective resin 70 as shown in Fig. 1I. After the protective resin 70 is cured, it is firm enough to support the elements therein. The copper sheet 10 is then etched away to expose the bottoms of the recesses 11, which now are downward round protrusions of the first electroplated layer 30 on the bottom of the resulting structure. Since the bottom sub-layer of the first electroplated layer 30 is nickel, the first electroplated layer 30 will not be etched by the etchant used in copper etching. Therefore, the copper sheet 10 can be completely removed without damage to the first electroplated layer 30.

With Reference to Fig. 1J, the bottom of the resulting structure is then covered with a patterned green paint 80 that exposes the downward protrusions of the first electroplated layer 30 serving as the external contact positions. The green paint 80 is patterned in a photosensitive way similar to the exposure/development techniques applied to the dry films 20, 40 and 41.

A sub-layer, i.e. a nickel layer, on the top of the protrusions of the first electroplated layer 30 is then removed to expose the next sub-layer, i.e. a gold layer, as shown in Fig. 1K, thereby finishing the BGA IC package.

As described above, the copper sheet 10 is temporarily used as a supporting plate to carry the chip 60. After the chip 60 is sealed with a resin, the copper sheet 10 can be etched away, reducing the thickness of the BGA package. Further, the first electroplated layer 30 is used as the external contact positions that are securely embedded in the BGA package, eliminating the use of solder balls that are poor in attachment and tensile strength.

It is to be understood, however, that even though numerous characteristics and advantages of the present invention have been set forth in the foregoing description, together with details of the structure and function of the invention, the disclosure is illustrative only, and changes may be made in detail, especially in matters of shape, size, and arrangement of parts within the principles of the invention to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.

CLAIMS

1. A packaging method for a ball grid array (BGA) integrated circuit (IC) without utilizing a base plate and solder balls, comprising the steps of:

covering a copper sheet with a first patterned dry film that will assist in forming external contact positions of said BGA IC;

slightly etching the surface of said copper sheet uncovered with said first patterned dry film to form substantially round recesses;

electroplating said recesses with metal to form a first electroplated layer covering said recesses;

removing said first dry film;

covering the top of said copper sheet with a second patterned dry film that corresponds to desired circuit areas and exposes the central portion of said copper sheet and all of said first electroplated layer;

electroplating said central portion of said copper sheet and all of said first electroplated layer with metal to form a second electroplated layer;

covering the top of the resulting structure with a third patterned dry film that exposes a desired bond pad area;

electroplating said bond pad area with metal to form a third electroplated layer;

removing said second and third dry films;

implanting an IC chip on said central portion of said copper sheet, electrically connecting the terminals of said chip with said bond pad area by wires and sealing said chip and wires with a resin;

etching said copper sheet to expose the bottoms of said recesses that are the downward protrusions of said first electroplated layer; and

covering the bottom of the resulting structure with a patterned green paint that exposes said protrusions of said first electroplated layer serving as said external contact positions,

thereby packaging said BGA IC without utilizing a base plate and solder balls.

2. The method according to claim 1, wherein said first electroplated layer consists in sequence of nickel, gold, nickel and tin, from the bottom to the top.

3. The method according to claim 1 or 2, after said step of covering the bottom of the resulting structure with said patterned green paint, further comprises a step of removing a sub-layer in said first electroplated layer.

4. The method according to claim 3, wherein said sub-layer is a nickel layer.

5. The method according to claim 1, wherein said second electroplated layer consists of nickel, copper and gold.

6. The method according to claim 1, wherein said third electroplated layer consists of gold.

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(54)名稱：免基板及免錫球之球陣式積體電路封裝方法

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[57]申請專利範圍：

1.一種免基板及免錫球之球陣式積體電路封裝方法，包括：

一為任銅片上覆蓋供形成外部接點之乾膜，並為對未被乾膜覆蓋之銅片表面進施以略微蝕刻，以形成概略呈圓凹槽之步驟；

一對該各凹槽部位施以電鍍，而形成覆蓋在各個凹槽內之圓粒狀第一電鍍層之步驟；

一去除前述乾膜之步驟；

一覆蓋線路乾膜，而對銅片中央部位以及對應於前述覆蓋第一電鍍層之上方電鍍形成第二電鍍層之步驟；

一再行覆蓋另一可使焊墊區外露之乾膜以反對該焊墊區進行電鍍形成第三電鍍層的步驟；

一去除前述各層乾膜之步驟；

一植入晶片、打線及封膠之步驟；及

一蝕刻底面銅片，而使各個第一電鍍層之底面外露與一覆綠漆之步驟；

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藉以構成一不含基板及無需植入錫球之球陣式積體電路封裝者。

2.如申請專利範圍第1項所述之免基板及免錫球之球陣式積體電路封裝方法，其中該第一電鍍層由下至上依序為以鎳、金、鎳、銅等材料組成而成者。

3.如申請專利範圍第1或2項所述之免基板及免錫球之球陣式積體電路封裝方法，其中該覆綠漆之步驟後，更包括一剝離第一電鍍層局部材料層之步驟。

4.如申請專利範圍第3項所述之免基板及免錫球之球陣式積體電路封裝方法，其中該被剝離之材料層為鎳者。

5.如申請專利範圍第1項所述之免基板及免錫球之球陣式積體電路封裝方法，其中該第二電鍍層為以鎳、銅材料組合而成。

6.如申請專利範圍第1項所述之免基板及免錫球之球陣式積體電路封裝方法，其中該第三電鍍層為金。

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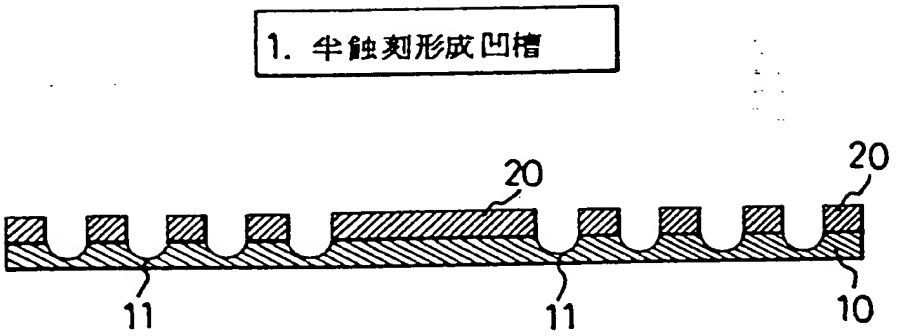
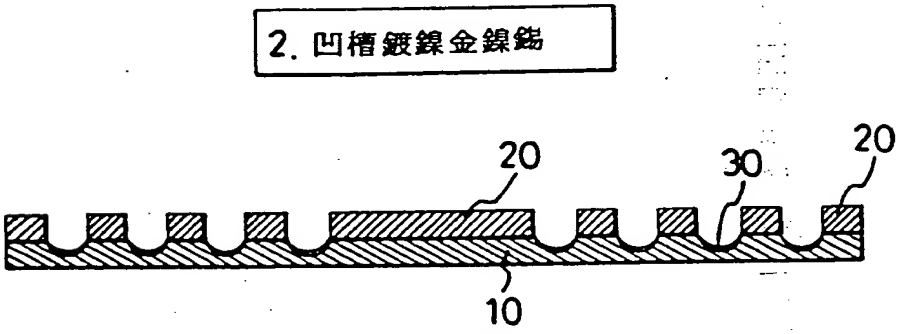
圖式簡單說明：

法步驟示意圖。

第一圖A～第一圖K：係本發明之方



第一圖 A



第一圖 B

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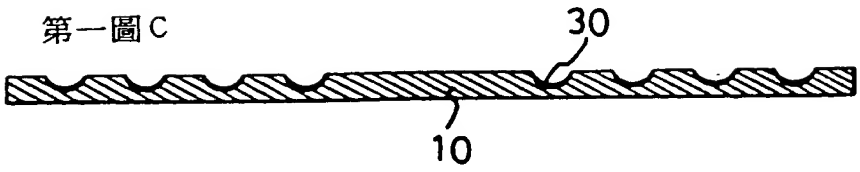
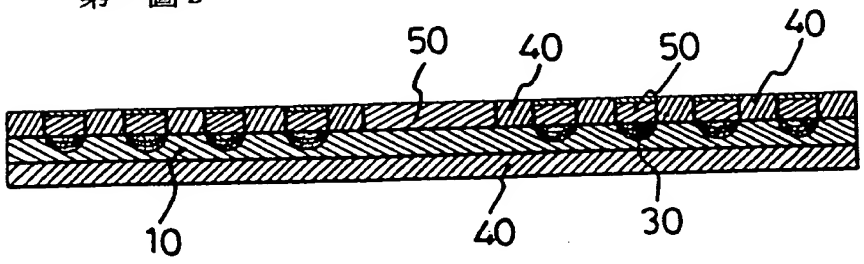
3. 去膜

第一圖 C



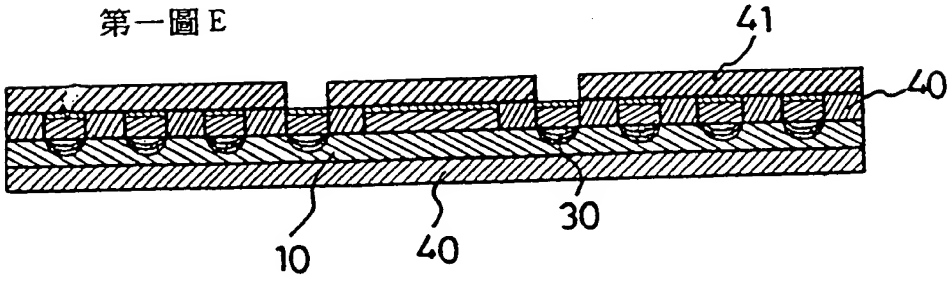
4. 線路區鍍錫銅金

第一圖 D



5. 鍍膜

第一圖 E



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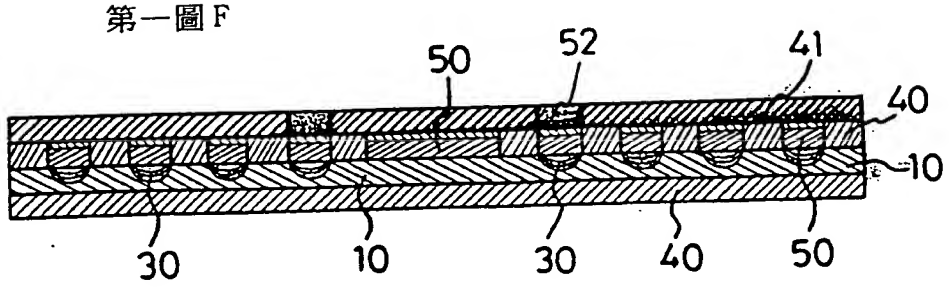
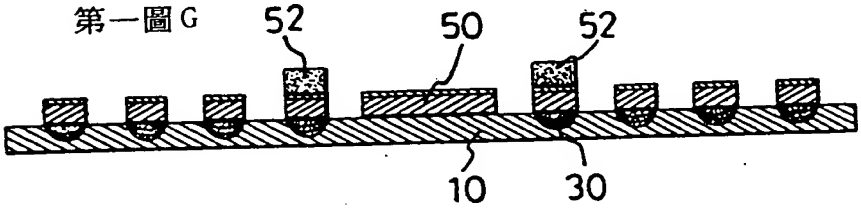
6. 焊墊區鍍金

第一圖 F



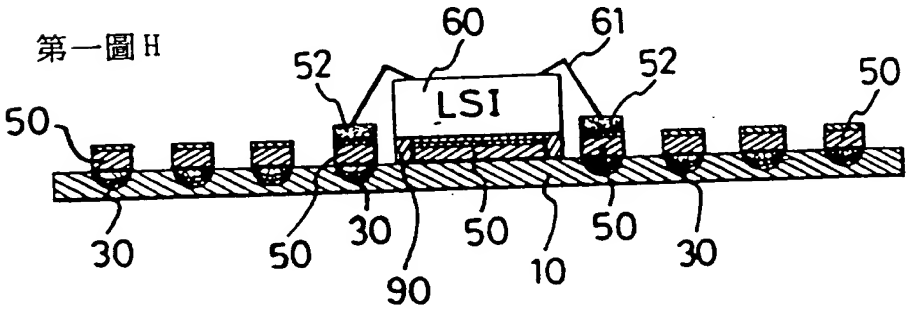
7. 去膜

第一圖 G



8. 植晶片打線

第一圖 H



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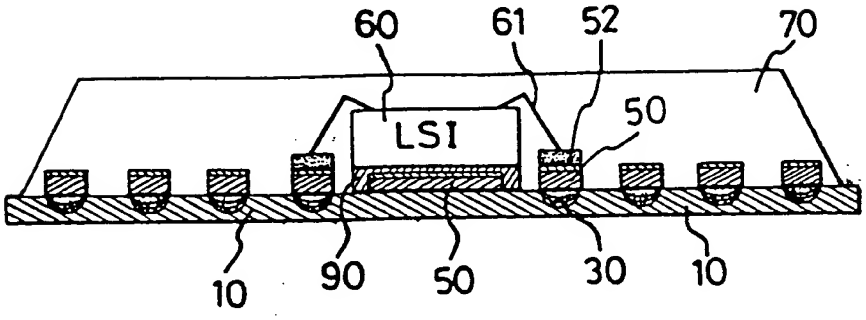
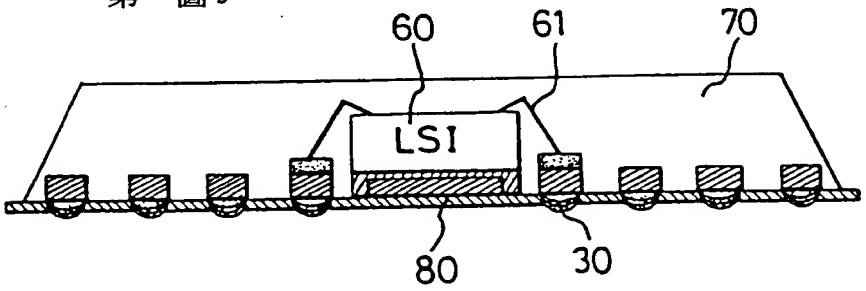
9. 封膠

第一圖 I



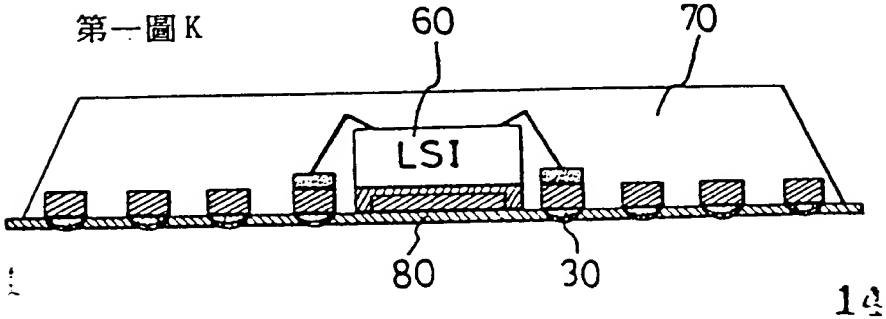
10. 蝕銅作絲漆

第一圖 J



11. 剝錄

第一圖 K



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公告本

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（以上各欄由本局填註）

340297

發明 新型 專利說明書

一、發明新型名稱	中文	免基板及免錫球之球陣式積體電路封裝方法（修正本）
	英文	
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	住、居所（事務所）	桃園縣蘆竹鄉新莊村大新路814巷91號
	代表人姓名	吳健

五、發明說明（ ）

本發明係為一種免基板及免錫球之球陣式積體電路封裝方法，為一種無需使用基板及無錫球之球陣式（ＢＧＡ）積體電路的封裝方法，達到使外包裝更趨小巧以及提供較佳的結構強度者。

按現今積體電路外包裝型態為達到符合不同場合的需要，即有各式不同的外包裝，諸如ＤＩＰ、ＰＧＡ、ＢＧＡ、ＴＡＢ……等型式，以球陣式（ＢＧＡ）(BALL GRID ARRAY) 積體電路的外包裝而論，即為在積體電路外包裝的底面形成縱橫排列的多數錫球接點，而供熱熔焊接於電路板相應之接點上者，然以此等包裝型態下，由於受到製程期間需適當支撐以及供做為錫球與晶片之介質之下，一般均需以電路板做為『支撐基板』，然以加入基板之封裝型態上，即導致外包裝尺寸厚度增加，此舉，對於包裝尺寸要求較為嚴苛的筆記型或次筆記型電腦上使用時，即有過於佔用空間之問題存在，再者，該附著於底面之錫球亦為一種外加的型態，其所提供之結構強度亦不足夠，於受到較大拉力作用下，當有著易導致錫球剝落之缺陷，亦有一併加以改進之必要。

本發明人鑑於現今ＢＧＡ封裝所衍生之厚度較厚以及透過錫球連接所衍生之結構強度不足之缺失下，乃經悉心地試驗與研究並一本鍥而不捨之發明精神，終發明出一種免基板及免錫球之球陣式積體電路封裝方法，亦即為形成一種內部無基板及無需附加錫球之球陣式積體電路外包裝

五、發明說明（～）

型態，藉省略基板而使得外包裝更趨輕薄短小，另透過封裝製程期間以電鍍形成電鍍凸點以達到相同於傳統錫球之作用，藉此電鍍凸點為嵌入於內部之型態下，獲致提昇接點機械強度者。

本發明之主要目的在於提供一種免基板及免錫球之球陣式積體電路封裝方法，封裝方式上主要為預先在一銅片上經覆乾膜與經半蝕刻步驟，而在銅片上形成接點凹槽，其次，於凹槽位置電鍍形成第一電鍍層（供做為接點使用），然後，為經去除乾膜與覆蓋另一乾膜後，即對應於各個第一電鍍層位置上方電鍍形成向上凸起之第二電鍍層，其次，則為在供黏著晶片之外圍位置的焊墊部位施以電鍍步驟後，即可依序進行植晶片、打線及封膠步驟，最後，則為蝕刻去除底面位置之銅片而僅留下該外突之第一電鍍層以及進行覆綠漆之步驟後，即完成封裝步驟，在上述步驟中，即藉由先前之銅片做為製程期間之支撐，而使其內部呈無基板之輕巧的包裝型式，且由於該第一電鍍層為在製程期間一併形成穩固嵌入在內部之型態，更無傳統錫球接點之易剝落與結構強度不足之問題。

為使　貴審查委員能進一步瞭解本發明之方法，特徵及其他目的，茲　附以圖式詳細說明如后：

（一）．圖式部份：

第一A～K圖：係本發明之方法步驟示意圖。

（二）．圖號部份：

五、發明說明（ 7 ）

（１０）銅片　　（１１）凹槽

（２０）（４０）（４１）乾膜

（３０）（５０）（５２）電鍍層

（６０）晶片　　（６１）金線

（７０）保護膠　　（８０）綠漆

（９０）銀膠

本發明可使最終成品可獲致無基板及免錫球型式之封裝方法上，概為如第一Ａ～Ｋ圖所示，首先為在第一Ａ圖之銅片（１０）上經覆蓋乾膜（２０）與對該未被乾膜（２０）遮蔽之位置進行半蝕刻之步驟，此半蝕刻步驟亦即為對銅片（１０）進行些微的蝕刻作業，而使得銅片（１０）上形成多數的凹槽（１１），而各凹槽（１１）所在位置即為外接接點之部位（容後詳述），其次，為如第一Ｂ圖所示，亦為透過先前之乾膜（２０）而對各凹槽（１１）位置進行依序進行鍍鎳、鍍金、鍍鎳及鍍錫而形成具有多層材料所組成之第一電鍍層（３０），而在第一Ｃ圖去除該前述乾膜（２０）後，則另於第一Ｄ圖中，覆蓋另一線路乾膜（４０），而此線路乾膜（４０）僅覆蓋在各個第一電鍍層（３０）之間的位置上，然後再以此線路乾膜（４０）做為遮罩，而於銅片（１０）之中央位置以及對應於各個第一電鍍層（３０）的上方位置以及線路部位形成向上突伸之第二電鍍層（５０）（此電鍍層為以鎳、銅及金材料所組成），然後，為如第一Ｅ圖所示，於不去

五、發明說明（ㄐ）

除該乾膜（４０）的狀態下，更覆蓋另一乾膜（４１），而僅於中央兩側位置之供做為晶片之焊墊(BOND PAD)部位形成開口，並在第一Ｆ圖中對該焊墊區進行鍍金之步驟，以形成填滿該開口部位之第三電鍍層（５２），故而在第一Ｇ圖中經去除前述兩乾膜（４１）（４０）後，即可進行如第一Ｈ圖之為由中央向上凸起之第二電鍍層（５０）位置經覆蓋銀膠（９０）、黏著晶片（６０）及對晶片（６０）與外圍之焊墊區所形成之第三電鍍層（５２）之間進行打金線（６１）之步驟，然後為如第一Ｉ圖所示，為在外表面覆蓋保護膠（７０）之封膠步驟後，即概略形成一積體電路封裝，此時，該保護膠（７０）經成型後更為形成一種質地堅硬的型態，具有支撐此封裝之作用，最後，為如第一Ｊ圖中，為蝕刻去除位在底面之銅片（１０）以及進行上綠漆（８０）之步驟，在此步驟中，由於該第一電鍍層（３０）的底層材料為鎳金屬，為不致遭蝕銅溶液蝕刻之故，因此，僅完全去除底部之銅片（１０）而不致損及第一電鍍層（３０），該上綠漆（８０）的步驟，為使用感光型綠漆，透過類似於乾膜之曝光／顯影的步驟，而使第一電鍍層（３０）呈外露而不致遭綠漆（８０）覆蓋，於上述製程完成後，則在底面位置僅留下該先前形成之向下突出的第一電鍍層（３０），最後，則為如第一Ｋ圖所示，經剝離附著在該各個外露之第一電鍍層（３０）表面之鎳材料，使其內部之鍍金材料外露後，即完成整

五、發明說明（ 5 ）

個封裝流程。

而在前述封裝作業期間，即運用該銅片（１０）做為中間流程之機械支撐，惟在經灌膠後，即可藉由保護膠（７０）提供應有的支撐強度，因此，在後續步驟中，則可直接將該銅片（１０）蝕刻去除，而形成一種完全不含支撐基板的ＢＧＡ積體電路包裝者，如此，當有降低包裝厚度與使得外包裝更趨輕薄小巧之功效，並由前述本發明之最終成品（如第一Ｋ圖）觀之，各個由底面外露之第一電鍍層（３０）為一種嵌入於內部之型態，此等型態與傳統外加錫球之方式相較，更有提昇接點部位機械強度及提供較佳的抗拉強度者，當為一較傳統製程更為進步之設計。

而就製法之技術特徵而論，除了透過前述銅片做為製程期間之支撐之外，更巧妙地對銅片（１０）進行半蝕刻形成凹槽（１１），於凹槽（１１）中電鍍形成呈半圓粒狀之第一電鍍層，使其在後續蝕刻去除該銅片（１０）之後，為呈圓粒狀之第一電鍍層外露及充做為外部接點使用，其封裝方法更具創意及巧思，為為一確具新穎性及進步性之球陣式積體電路封裝方法，應符專利申請要件，爰依法提出申請。

A5
B5

四、中文發明摘要（發明之名稱：　　）

免基板及免錫球之球陣式積體電路封裝方法

本發明係關於一種免基板及免錫球之球陣式積體電路封裝方法，尤指一種無需使用導線架(lead frame)為基材以及無須進行植入錫球之球陣式積體電路封裝，達到令外包裝更趨輕薄短小，並解決錫球強度不足之缺陷，主要為在銅片上經覆乾膜與半蝕刻步驟，而在銅片上形成供做為後續接點使用之凹槽，其次，為在凹槽位置形成第一電鍍層（供接點使用），然後為依序進行去除乾膜、覆另一乾膜與電鍍之步驟，以形成由各個凹槽向上凸伸之內部接點，而后，為對焊墊區進行電鍍之步驟、植晶片、打線、封膠、蝕刻去除最下方之銅片與覆蓋綠漆之後，即形成一種可藉前述成型之第一電鍍層做為外部接點，而內部無基板之積體電路封裝。

英文發明摘要（發明之名稱：　　）

六、申請專利範圍

1．一種免基板及免錫球之球陣式積體電路封裝方法，包括：

一為在銅片上覆蓋供形成外部接點之乾膜，並為對未被乾膜覆蓋之銅片表面進施以略微蝕刻，以形成概略呈圓凹槽之步驟；

一對該各凹槽部位施以電鍍，而形成覆蓋在各個凹槽內之圓粒狀第一電鍍層之步驟；

一去除前述乾膜之步驟；

一覆蓋線路乾膜，而對銅片中央部位以及對應於前述覆蓋第一電鍍層之上方電鍍形成第二電鍍層之步驟；

一再行覆蓋另一可使焊墊區外露之乾膜以及對該焊墊區進行電鍍形成第三電鍍層的步驟；

一去除前述各層乾膜之步驟；

一植入晶片、打線及封膠之步驟；及

一蝕刻底面銅片，而使各個第一電鍍層之底面外露與一覆綠漆之步驟；

藉以構成一不含基板及無需植入錫球之球陣式積體電路封裝者。

2．如申請專利範圍第1項所述之免基板及免錫球之球陣式積體電路封裝方法，其中該第一電鍍層由下至上依序為以鎳、金、鎳、銅等材料組成而成者。

3．如申請專利範圍第1或2項所述之免基板及免錫球之球陣式積體電路封裝方法，其中該覆綠漆之步驟後，

六、申請專利範圍

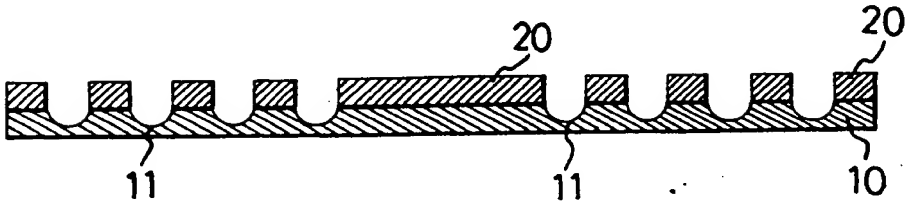
更包括一剝離第一電鍍層局部材料層之步驟。

4．如申請專利範圍第3項所述之免基板及免錫球之球陣式積體電路封裝方法，其中該被剝離之材料層為鎳者。

5．如申請專利範圍第1項所述之免基板及免錫球之球陣式積體電路封裝方法，其中該第二電鍍層為以鎳、銅材料組合而成。

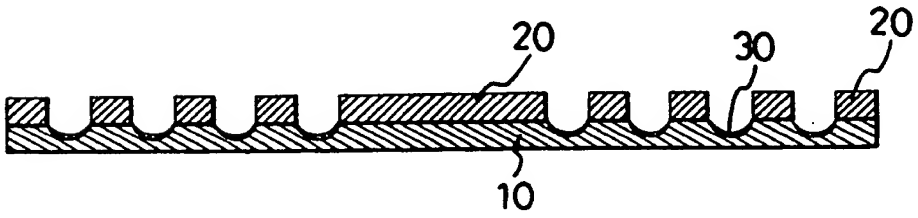
6．如申請專利範圍第1項所述之免基板及免錫球之球陣式積體電路封裝方法，其中該第三電鍍層為金。

1. 半蝕刻形成凹槽



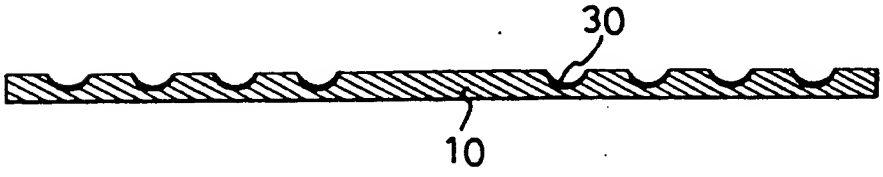
第一A圖

2. 凹槽鍍鎳金鎳錫



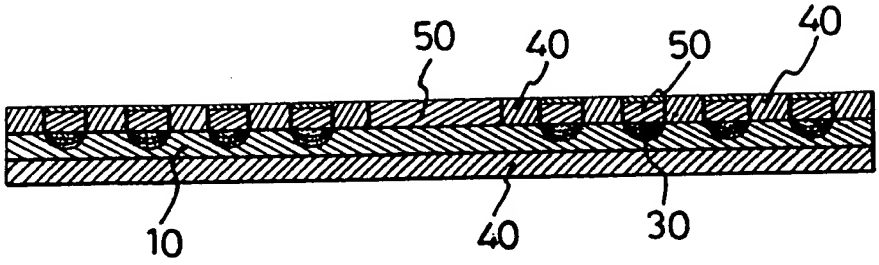
第一B圖

3. 去膜



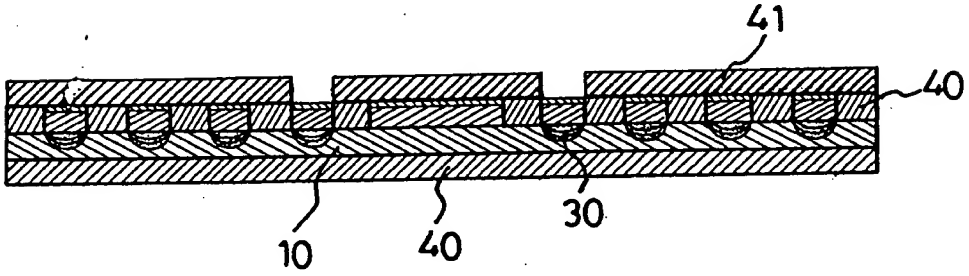
第一C圖

4. 線路區鍍錫銅金



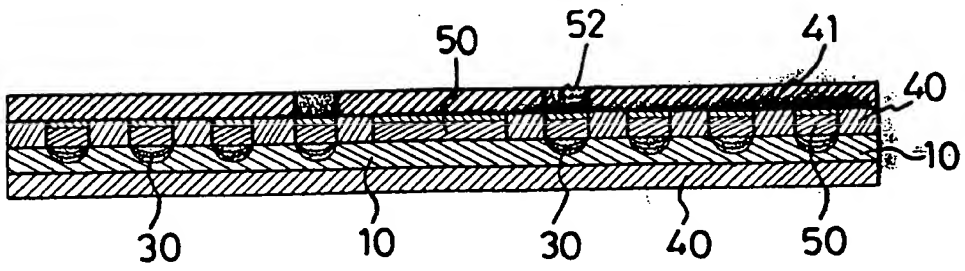
第一D圖

5. 覆膜



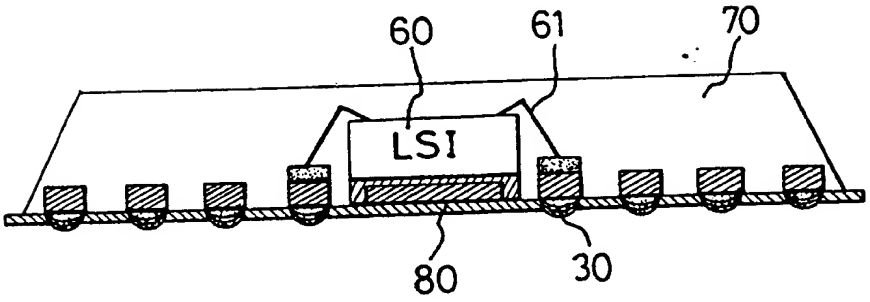
第一E圖

6. 焊墊區鍍金



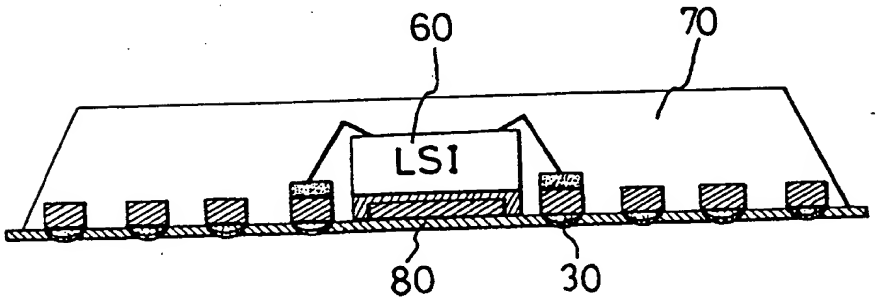
第一F圖

10. 蝕銅作綠漆



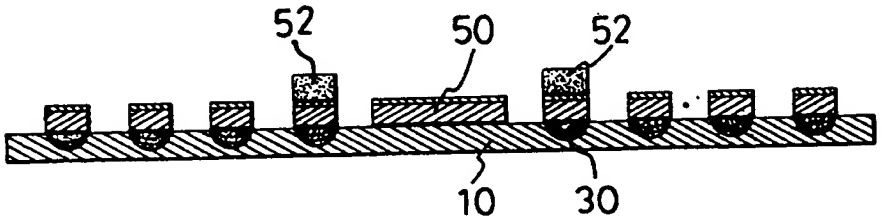
第一J圖

11. 剝錄



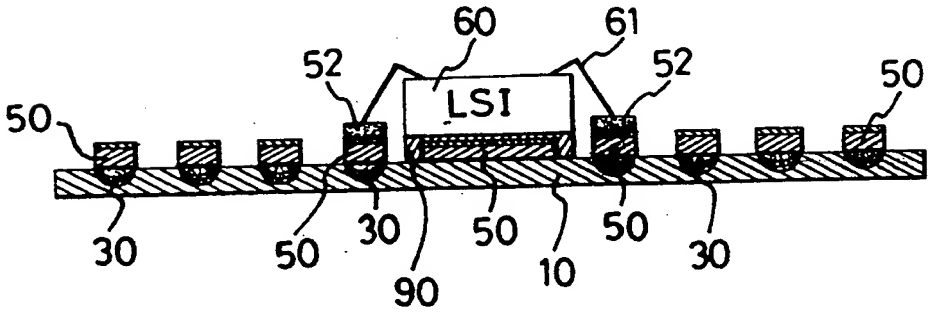
第一K圖

7. 去膜



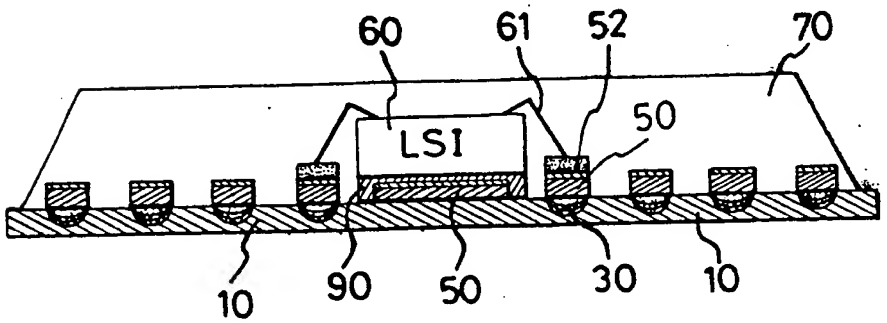
第一G圖

8. 植晶片打線



第一H圖

9. 封膠



第一I圖